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Impact of PCB Layout Design on Final Product's EMI Compliance

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Abstract — Most design engineers still believe that with a good shielded enclosure, well-shielded cables and high-performance ferrite sleeves, EMI compliance will be a straight forward task. This paper demonstrates experimentally that a poor PCB layout can cause electronic product to fail EMI specification badly even with all these fixes.

I. INTRODUCTION

With the trend of increasing speed and complexity, meeting EMI requirements is no longer a simple task. There could be several sources of EMI at system and subsystem levels. And these sources of EMI cannot be identified just by doing a final product EMI testing. To ensure that the final product meets the stringent EMI requirement, proper EMI suppression techniques must be implemented at the subsystem levels, rather than relying on final fixes, such as adding shields, filters and ferrite sleeves.

Unfortunately, most design engineers still buy the ideas of leaving EMC design at the last stage of product development. They expect the typical fixes to solve all the EMI problems at the final product testing stage. Using a realistic replicate of a typical electronic product, the authors will like to demonstrate that the last-minute fixes can do very little if the subsystem, for example, a

high-speed PCB, is designed without any EMI consideration.

II. GENERIC ELECTRONIC PRODUCT

A generic electronic product, as shown in Fig. 1, is designed and fabricated[1]. Like any typical electronic products, it has an AC inlet for AC power supply. The AC power is converted to low voltage DC power through a switched-mode power supply (SMPS). The DC power is then fed to a printed circuit board (PCB) that holds high-speed digital circuitry shown in Fig. 2. The high-speed digital circuitry is supplied by 5V and operates at 25MHz clock. Output port of the PCB is interfaced with an external PCB, which contains resistive load, by a 1.5m shielded cable. Finally, the PCB and SMPS is packaged into a well-shielded[2] metallic enclosure of size 30cm x 22cm x 12cm.

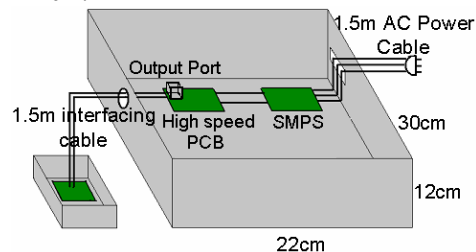


Fig. 1. Complete Digital Electronic System

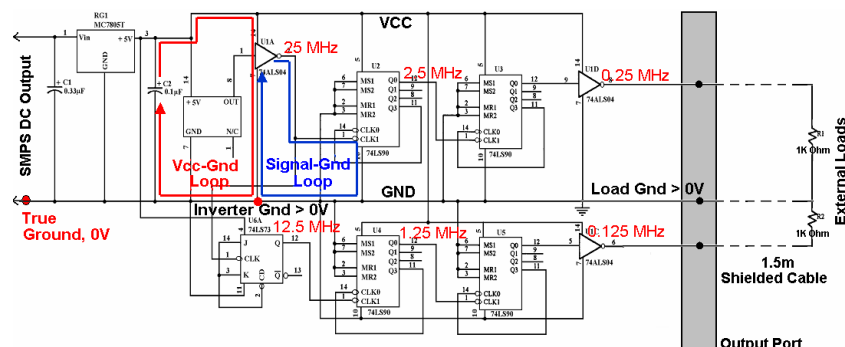
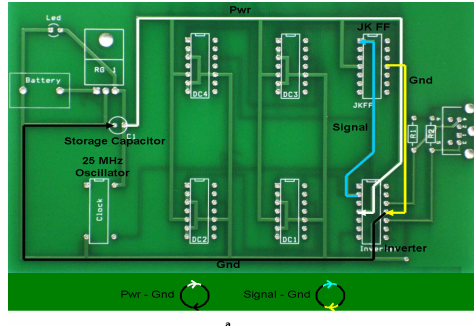


Fig. 2. Digital Circuitry Operating at 25 MHz Clock

III. EMI MEASUREMENT RESULTS

Fig. 3a shows the first PCB layout of the digital circuit. It is a single-layer doubled-sided board with power and signal traces routed on one side and the ground traces routed on another side. The traces are far apart and result in large power-to-ground and signal-



to-ground loops[3-5], as indicated in Fig. 3a. Fig. 3b shows radiated emissions from this PCB after powered by the SMPS. The measurement is done with no interfacing cable and no shielded enclosure. As expected, due to poor PCB's layout without EMI consideration, radiated emissions have exceeded CISPR 22 Class B limit badly by as much as 30 dB at some frequencies.

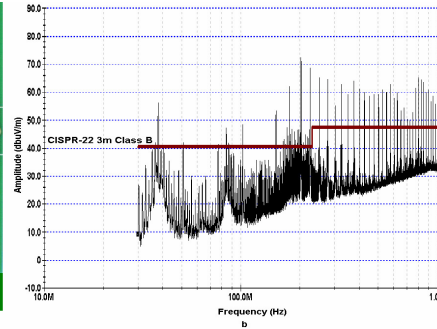


Fig. 3. (a) Poor PCB Layout; (b) Radiated Emissions Result

Fig. 4a shows the SMPS and PCB housed in a well-designed shielded box with all its edges lined with conductive CuBe gaskets. A good shielded cable with a clamp-on type ferrite sleeve is used to interface PCB's output port with an external board that consists of $1\text{K}\Omega$ resistors for termination purposes. With all these so called "good and effective" fixes, one would expect radiated emissions from the final assembled product to meet CISPR 22 Class B limit. However, Fig. 5a shows that radiated emissions from the final assembled product still fails to comply with the limit inspite of well shielded casing, well shielded cable and

high-attenuation ferrite sleeve. It clearly indicates that all these expensive fixes do not guarantee EMI compliance if the PCB is poorly designed. The cause of the failure is due to excessive radiation from poor PCB and common-mode (CM) radiation from the interfacing cable[6]. The CM current measured using a current probe reveals that the level of CM current is very high due to large ground bounce at the output port. Measured CM current on the interfacing cable and ground potential between the PCB output port and DC power's 0V reference are shown in Fig. 5a and Fig. 5b, respectively.

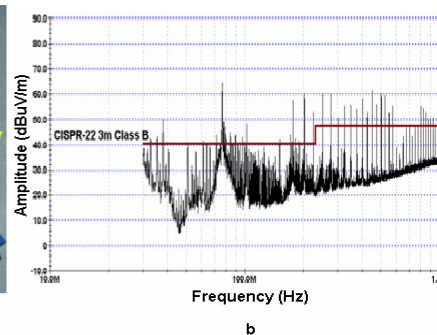
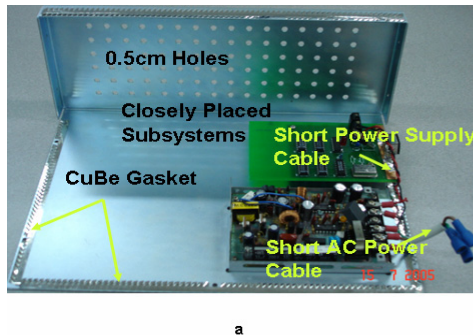


Fig. 4. (a) Final Assembled Electronic System; (b) Radiated Emissions Result

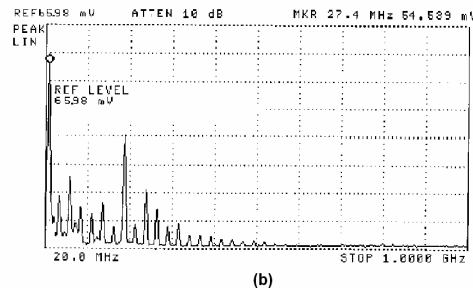
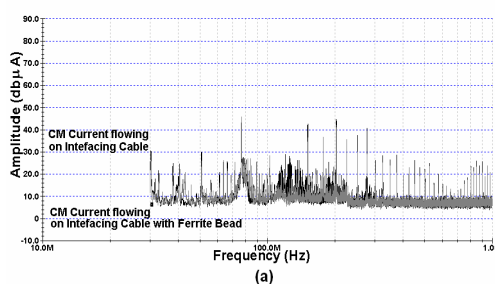


Fig. 5. (a) CM Current flowing through the Cable; (b) Ground Bounce at the Output Port

To reduce radiated emissions from the PCB, a new layout with EMI consideration is designed. Fig. 6a shows the new PCB layout of the digital circuit. It is a single-layer doubled-sided board with one side dedicated as a ground plane and the other side for power and signal traces. The ground plane helps to reduce sizes of power-to-ground and signal-to-ground loops significantly[7-8]. To further reduce the loop areas, IC gates and components are placed close

together. Radiated emissions from the well-designed PCB layout is shown in Fig. 6b, they are below CISPR22 Class B limit[9]. However, after attaching the interfacing cable, radiated emissions have exceeded the limit. To reduce the CM radiation, 5nF bypass capacitor and ferrite bead are added at the output port of the PCB. Fig. 7 shows that implemented solution has lowered radiation level by as much as 15dB.

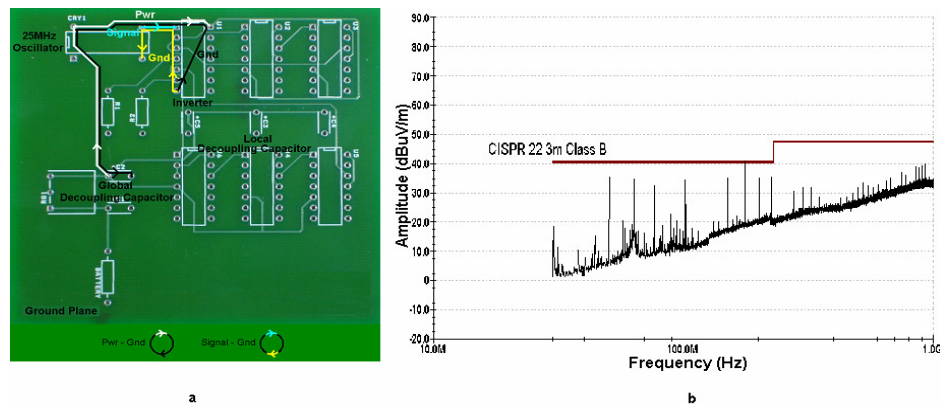


Fig. 6. (a) Well Designed PCB Layout; (b) Radiated Emission from Well Designed PCB

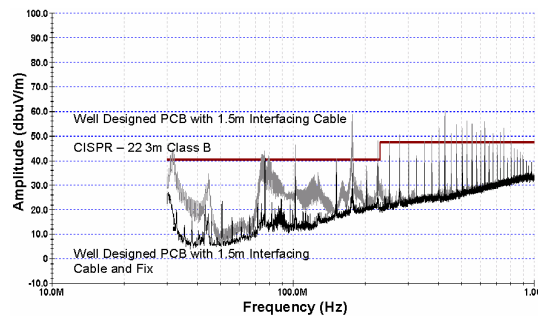


Fig. 7. Radiated Emissions from Well Designed PCB with Interfacing Cable and with Fixes

Finally, the PCB and SMPS are housed in the well shielded casing. Radiated emissions from the final assembled product are measured. Fig. 8 shows radiated emissions from the assembled product with two different PCB layouts. Assembled product with the well designed PCB layout has met the CISPR 22 Class B limit with very good margin. It shows that the new

PCB layout has substantially reduced the CM radiation from the interfacing cable and well-designed PCB itself radiates significantly less. Fig. 9 shows the measured CM current on the cable and the ground bounce of the output port of the PCB. Both the CM current and ground bounce are much lower as compared to those shown in Figs 5(a) & 5(b).

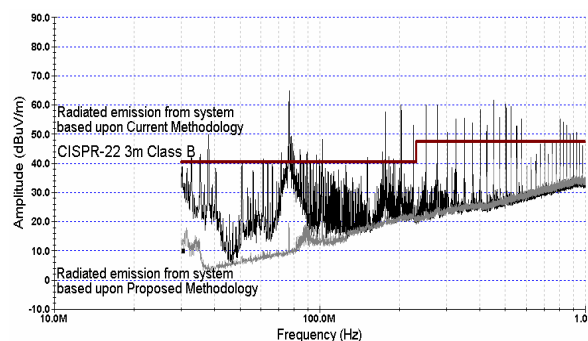


Fig. 8. Comparison between assembled systems with Well-designed and Poor PCB layouts

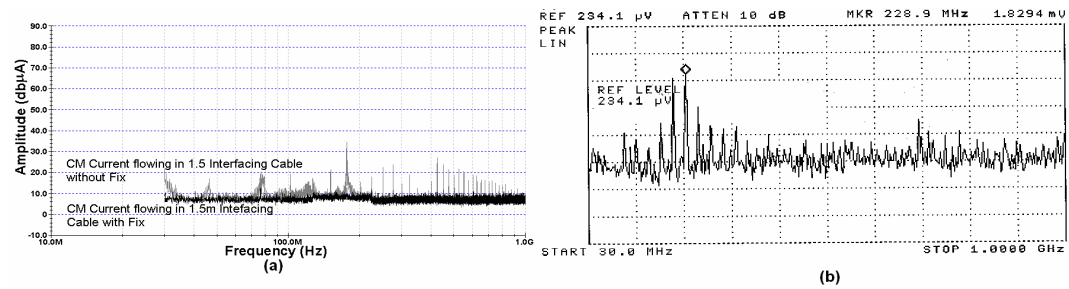


Fig. 9. (a) CM Current on the Cable; (b) Ground Bounce of the Output Port

IV. CONCLUSION

With a realistic prototype of an electronic product, it is demonstrated that PCB layout design plays a crucial role for final product's EMI compliance. The layout decides the level of ground bounce at the output port of the PCB, which is the major cause of CM radiation through interfacing cable. Excessive ground bounce due to poor PCB layout leads to significant level of CM radiation and in addition to emission from PCB has a direct impact on product's EMI compliance. Even expensive shielded enclosure, shielded cable and ferrite sleeves are ineffective to control CM radiation substantially to meet the EMI specification. Careful designing of PCB layout with EMI consideration can reduce EMI issues at system level hence EMC compliance can be achieved easily.

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